REMARKS

Claims 10, 15, and 17 have been canceled. Claims 1, 9, and 13 have been amended. Claims 21 – 23 have been added. Claims 1-9, 11-14, 16-23 are currently pending in the present application. No new matter has been added. Reexamination and reconsideration of the application are respectfully requested.

REJECTION OF CLAIMS 1-20 UNDER 35 U.S.C. 103(a)

Claims 1-20 are rejected under 35 U.S.C. 103 for the reasons set forth on pages 2-4 of the Action. Specifically, claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda (U.S. Pat. No. 5,832,281, hereinafter referred to as "Maeda" or "the Maeda reference") in view of Hidehiko et al. (JP 06052070A, hereinafter referred to as "Hidehiko" or "the Hidehiko reference").

Regarding claim 1, the Action asserts that the elements 6, 11, 29, 38, 39, 50 of Maeda discloses the claimed invention, except for teaching "the state save being a scan-based state save." The Hidehiko reference is cited for teaching "the use of a scan-based state-save and restore of data in a circuit upon power source discontinuation." The Action further states that it would have been obvious to a person of ordinary skill in the art at the time the invention to "use state-save in Maeda because this would have provided a fast method of data evacuation."

The rejections under 35 U.S.C. 103 are respectfully traversed, at least insofar as applied to the new and amended claims, and reconsideration and reexamination of the application is respectfully requested for the reasons set forth hereinbelow.

The Action on page 2 proposes a combination of Maeda's power control apparatus with the device and method for data protection in integrated circuits set forth by the Hidehiko reference. This combination is contested as improper for the reasons advanced below. However, even if this combination were proper, which is not conceded, the resulting combination would still fail to teach or suggest the claimed invention.

THE PROPOSED COMBINATION IS BASED ON IMPERMISSIBLE USE OF THE CLAIMED INVENTION AS A TEMPLATE TO PIECE TOGETHER THE TEACHINGS OF THE MAEDA REFERENCE AND THE HIDEHIKO REFERENCE

It is respectfully submitted that the Maeda and Hidehiko references are improperly combined. It appears that the Action uses improper hindsight to selectively pick circuit elements from Maeda and techniques from Hidehiko to arrive at the claimed invention.

First, it is respectfully submitted that the Maeda reference does not explicitly or implicitly teach or suggest any motivation to combine the Maeda reference with the Hidehiko reference or any motivation to modify the Maeda's power control apparatus and method with the data protection scheme of the Hidehiko reference.

The Action suggests that the power control apparatus of Maeda utilize the data transfer technique taught by Hidehiko. However, the proposed combination teaches away from Maeda, which utilizes the hard disk (HDD) 15 to store "suspend data" (Maeda, col. 3, lines 56-60). As can be appreciated, the process used by Maeda to write

data to a hard disk is different from the process used by Hidehiko to write data to an external memory 3 by using a counter 4 and scan clock (SC). Furthermore, it is respectfully submitted that the proposed combination does not appear to be enabled by the disclosure of the cited references.

Assuming arguendo that the data transfer technique of Hikehiko can somehow be incorporated into the power control apparatus of Maeda, the Federal Circuit has stated, "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d 1260, 23 USPQ 2d 1780, 1783–84 (Fed. Cir. 1992) [emphasis added].

The Federal Circuit has further held In re Fritch, 972 F.2d 1260, 23 USPQ 2d 1780, 1783 (Fed. Cir. 1992):

> In proceedings before the Patent and Trademark Office, the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art. ... "[The Examiner] can satisfy this burden only by showing some objective teaching in the prior art ... would lead that individual to combine the relevant teachings of the references. In re Fine, 837 F.2d 1071, 1074, 5 USPQ 2d 1596, 1598 (Fed. Cir. 1988). [emphasis added.]

The Action on page 2 cites, "using a scan-based state save in Maeda because this would have provided a fast method of data evacuation," as the motivation to combine the teachings of the Maeda reference with selected disclosures from the Hidehiko reference.

Although both references are related to saving data as a general matter, it is respectfully submitted that the considerations in designing a data protection method and device of Hidehiko to save internal data of an integrated circuit to an external memory when power interruption occurs are different from the considerations for designing the power control apparatus of Maeda for recovering data destroyed due to erroneous user operation or battery exhaustion (col. 1, lines 31-60).

Consequently, it is respectfully suggested that this quoted portion from the Action is deficient and would not have motivated one of ordinary skill in the art to combine the pieces of information in the manner suggested by the Action.

Furthermore, even if Hidehiko fairly teaches and enables the use of a scan clock to save internal state data of an integrated circuit to an external memory, which is not conceded, this alone is not sufficient to render obvious the claimed invention since the use of a known scan-based technique in a new and non-obvious manner, for example, as applied to power reduction management, as claimed, is patentable.

Moreover, it is respectfully submitted that neither reference sets forth or addresses the specific problem addressed by the current invention as set forth in the application. It appears that the Hidehiko's technique is directed for protecting data loss in the event of failure or other power interruption. Maeda appears to be directed to an apparatus for recovering resume data destroyed because of user error or battery exhaustion (col. 1, lines 56-59). In sharp contrast, the invention as claimed provides power reduction management to address the problem of computing devices that use circuits that are manufactured with these sub-micron processes, where it is no longer

sufficient to simply stop the clock, but the chips must be completely disconnected from the power supply in order to conserve power as set forth in the specification. (Specification, pages 3-4)

Consequently, it appears that the current patent application has been improperly used as a basis for the motivation to combine or modify the components selected from Maeda and Hidehiko to arrive at the claimed invention. Stated differently, the proposed combination of the cited references appear to be based on hindsight since the cited references do not teach or suggest a motivation to combine the respective elements of each reference in the manner proposed by the Action.

The Federal Circuit has held, "It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated, "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." (quoting In re Fine, 837 F.2d 1071, 1075, 5 USPQ 2d 1596, 1600 (Fed. Cir. 1988)), In re Fritch, 23 USPQ 2d 1780, 1784 (Fed. Cir. 1992). [emphasis added.]

Furthermore, the Federal Circuit has held, "The combination of elements from non-analogous sources, in a manner that reconstructs the applicant's invention only with the benefit of hindsight, is insufficient to present a prima facie case of obviousness. There must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination. That

knowledge can not come from the applicant's invention itself." In re Oetiker, 977 F.2d 1443, 24 USPQ 2d 1443, 1446 (Fed. Cir. 1992)

Accordingly, hindsight reconstruction may not be used to pick a component from Maeda and another component from Hidehiko to arrive at the invention as claimed. Accordingly, it is respectfully requested that the rejection of claims 1-20 under 35 U.S.C. 103(a) be withdrawn.

In view of the foregoing, it is respectfully submitted that the Maeda reference, whether alone or in combination with the Hidehiko reference, fails to teach or suggest the circuit, circuit board, and method as claimed. Accordingly, it is respectfully requested that the claim rejections under 35 U.S.C. Section 103(a) be withdrawn.

EVEN IF PROPERLY COMBINED, THE MAEDA REFERENCE AND THE HIDEHIKO REFERENCE FAIL TO TEACH OR SUGGEST THE SPECIFIC LIMITATIONS SET FORTH BY THE INDEPENDENT AND DEPENDENT CLAIMS

It is respectfully submitted that even if the Maeda and Hidehiko references were properly combined, which is not conceded, Maeda, whether alone or in combination with Hidehiko, fails to teach or suggest specific limitation recited by the claims.

Specifically, Maeda, whether alone or in combination with Hidehiko, fails to teach or suggest "an inactive state power reduction manager .. for receiving a sleep signal and responsive thereto for asserting a stop clock signal to stop a normal mode clock, for performing a scan-based state-save", "b) stopping a normal mode clock; c) performing a state save by employing the scan circuitry," and "an inactive state power

reduction manager .. for receiving a sleep signal and responsive thereto for asserting a stop clock signal to stop a normal mode clock, for performing a scan-based state save of state information of the first integrated circuit and the second integrated circuit by using the test access port of the first integrated circuit and the second integrated circuit," as claimed in claims 1, 13, and 18, respectively.

The detection circuit 38 of Maeda does not fairly teach or suggest the inactive state power reduction manager as claimed because 1) detection circuit 38 generates different output signals and 2) operates in a very different manner than the inactive state power reduction manager as claimed. First, detection circuit 38 does not generate a stop clock signal and does not appear to stop any clock signal. Instead, detection circuit 38 utilizes a clock generator 39 to generate a clock signal (CLK) that is subsequently utilized for synchronization of control signals (see Maeda, col. 4, lines 22-31 and col. 5, lines 3-4, lines 35-39).

Furthermore, it does not appear that the clock signal (CLK) generated by clock generator 39 is every stopped. FIG. 9, which is a timing chart of the main signals in the detection circuit 38, supports this position. Specifically, FIG. 9 illustrates that the clock signal (CLK) (third waveform from the top) is constant, and its edges are utilized by other signals (e.g., the DC/DC - ON/OFF signal) for synchronization. In addition, the figures (e.g., FIG. 5-8) that illustrate the components of detection circuit 38 of FIG. 4 often show the CLK signal as a constant reference that is utilized to synchronize the logic implemented by the different blocks (e.g., 40, 41, 42, and 43). For example, FIG. 7, which illustrates in greater detail the switch interface 42 of FIG. 4, indicates that IC4

and IC5 each have a clock input that receives and is driven by the CLK signal, which serves as a reference signal needed for the correct operation of the flip-flops (IC4 and IC5). If the CLK signal of Maeda were to stop as suggested by the Action, the detection circuit 38 would not function in its intended manner. Consequently, detection circuit 38 of Maeda has very different output signals than the inactive state power reduction manager as claimed.

Moreover, it is noted that the clock generated by clock generator 39 (see FIG. 4) is not the same as the stop clock signal as claimed because, as advanced previously, the signal generated by clock generator 39 does not stop any clock signal.

It is noted that the dependent claims incorporate all the limitations of independent claims 1, 13, and 18, respectively. Furthermore, the dependent claims also add additional limitations, thereby making the dependent claims a fortiori and independently patentable over the cited references.

For example, dependent claims 21-23 recite limitations related to receiving a wake-up signal; responsive to the wake-up signal, re-connecting the switched power portion of the circuit to power; g) performing a state restore by employing the scan circuitry; and h) re-starting the normal mode clock. These limitations do not appear to be taught or suggested by the Maeda and Hidehiko references.

After a review of the cited references, there does not appear to be any teaching of the specific claims limitations recited by the dependent claims. In this regard, it is respectfully requested that the next Action specifically point out those portions of the

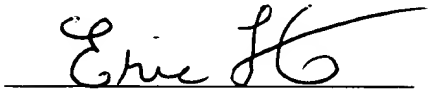
cited reference that teach or suggest the specific recited elements in the claimed invention.

In view of the foregoing, it is respectfully submitted that the Maeda reference, whether alone or in combination with the Hidehiko reference, fails to teach or suggest the circuit, method and system as claimed. Accordingly, it is respectfully requested that the claim rejections under 35 U.S.C. Section 103(a) be withdrawn.

Conclusion

For all the reasons advanced above, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the pending claims are requested, and allowance is earnestly solicited at an early date. The Examiner is invited to telephone the undersigned if the Examiner has any suggestions, thoughts or comments, which might expedite the prosecution of this case.

Respectfully submitted,



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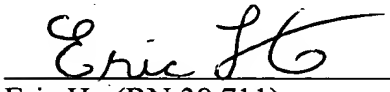

Eric Ho (RN 39,711) June 4, 2004 (Date)